Application dependent gate trigger requirements of GTO thyristors

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Abstract
The influence of the forward gate characteristics on the performance of Gate turn-off (GTO) thyristors in a range of practical applications including pulse power and voltage fed inverters is considered, with a series of experimental measurements being conducted on a wide ranging sample of test devices. The results obtained in experimental measurements are compared to those carried out in the normal rating procedure for this type of device and the optimised forward gating requirements of the GTO thyristor in a number of the applications is discussed.

Introduction
In most published material dealing with the operation and characterisation of GTO thyristors the principal consideration has been the turn-off. The introduction of some new applications and the increasing voltage of individual devices has brought a new emphasis to the turn-on characteristics. In particular the use of GTO thyristors as high current pulse switches, Bonthond et al [1], needs careful consideration of the turn-on characteristics for optimum performance. The application of GTO thyristors in series operation as [1] for pulse power or for HVDC requires close matching of the turn-on behaviour of the devices and any reduction in the spread in device characteristics by an appropriate gate drive, eases device selection. Individual devices with ever higher operating voltages are becoming available, but at the cost of increasing the turn-on voltage tail with the consequential increase in the turn-on loss, Evans.M et al [2], which may acquire a greater significance than the turn-off loss. An improved awareness of the significance of the forward gating characteristics of the GTO thyristor also prompts the reconsideration of the gating needs in some more traditional applications such as voltage fed inverters.

EXPERIMENTAL MEASUREMENTS.

Device Characterisation

Selection of the samples.
In order that the influence of the device characteristics was fully considered in the application based measurements a sample of GTO thyristors manufactured with a common silicon diameter and gate cathode structure were assembled. The sample included two different voltage grades of anode-shorted devices (2.5kV & 4.5kV) and three voltage grades of symmetrical devices (2.5kV, 3.6kV & 4.5kV), the devices having a nominal operational current of 800 amperes.

Measurement of the samples.
The devices were initially measured for trigger current and latching current across the full operating temperature range, along with the on-state voltage characteristic to ensure the sample included the full range of manufacturing variability.

Selected samples were measured for their turn-on characteristics using the standard production GTO thyristor tester employed at Westcode semiconductors to characterise devices. The full test circuit is quite complex and is primarily intended to evaluate the turn-off characteristics of the GTO thyristor, however, for the turn-on measurements the simple equivalent circuit given in figure 1 can be employed and the basic circuit operation is as follows. The required turn-on voltage is set, on the adjustable supply Vd, to charge capacitor Cc then thyristor T is fired and constant current is established in the thyristor loop. The constant current is supplied by PWM bi-polar transistor emitter switch and can supply current from 0 to 4000A. With Tx „on” the capacitor Cc is then charged to the same voltage as capacitor Cs minus the volt drop across Rs which is small. The GTO thyristor is then fired discharging Cc via Lc and at the same time commutating thyristor Tx „off” which redirects the constant current through the GTO thyristor. In combination with the supply voltage Vd, the values of Cs & Lc (adjustable in finite steps) are selected to give the desired peak current and anode di/dt respectively.

Figure 1, Turn-on test circuit.

The test circuit operation cycle requires the GTO thyristor to turn-off, therefore it is necessary to include a turn-off snubber. The turn-off snubber is of the simple RCD (resistor capacitor diode) type and comprises Ds, Rs & Cs in figure 1. When the test device (DUT) is turned on the capacitor Cc will discharge via Rs to limit the influence of this discharge the value of Rs was kept relatively high.

The gate drive circuit is of conventional type with parallel combinations of MOSFETs for both the „on” and „off” switches. The peak forward gate current (Igm) can be adjusted from 2 to 90A. The rate of rise of forward gate current (di/dt) is fixed by the inductance of the gate circuit which is in the same path as the turn-off circuit, limiting the range of adjustment.
Figure 2 gives the basic form of the turn-on wave-shapes obtained and includes the basic definitions of the parameters. The rate of rise of anode current \((\text{di/dt})\) and the rate of rise of gate current \((\text{di}_G/\text{dt})\) are defined as a cord from the 10% to 50% values of the final currents.

![Figure 2. Definition of turn-on parameters, as used throughout the paper.](image)

The test samples were characterised for turn-on delay time \((t_d)\), rise time \((t_r)\), voltage tail time \((t_{\text{tail}})\) and the corresponding turn-on energy in each phase was also recorded. The voltage tail time \((t_{\text{tail}})\) is measured from the end of the turn-on time \((t_o)\) to the point at which the voltage approaches the steady state voltage \((V_{\text{SS}})\). The principle test parameters considered for the measurements were the peak gate current \((I_{\text{GM}})\), rate of rise of anode current \((\text{di/dt})\), peak anode current \((I_{\text{TMM}})\) and anode to cathode line voltage \((V_D)\). The measured characteristics were each recorded against a range of the chosen principle test parameters. Due to the finite steps of \(C_c\) & \(L_c\) available in the test equipment some limitation in the selection of peak current and \(\text{di/dt}\) were experienced and this was reflected in the range of recorded results. Example results for a symmetrical 2.5kV device are included in the curves of figures 3 to 6, \((I_{\text{TMM}}=600\text{A} & \text{di/dt}=200\text{A/\mu s})\) in figures 3 & 4). The other device types mentioned earlier in the text yielded similar results to those of the sample device of the following graphical results.

![Figure 3. Turn-on time vs peak gate current.](image)

![Figure 4. Turn-on energy vs peak gate current.](image)

![Figure 5. Turn-on time vs \text{di/dt}.](image)

![Figure 6. Turn-on energy vs \text{di/dt}.](image)

**Analysis of results.**

During the characterisation of the test samples the following conclusions were drawn. The peak gate current \((I_{\text{GM}})\) shows an influence on the turn-on time and switching losses for all the sample types. The most noticeable change to the losses was seen in the 2.5kV devices, where the greatest contribution occurs in that part of the turn-on most influenced by the gate. Both delay time \((t_d)\) and rise time \((t_r)\) are influenced by the peak gate current \((I_{\text{GM}})\) with rise time \((t_r)\) being the most effected. In general delay time \((t_d)\) is only increased at peak gate currents \((I_{\text{GM}})\) below 20 amperes, were as the rise time \((t_r)\) did not reach a minimum value until the peak gate current \((I_{\text{GM}})\) reached 50 amperes in some of the samples.

The influence of the peak gate current \((I_{\text{GM}})\) on the total losses at turn-on \((E_{\text{on}})\) is similar to that found in the turn-on time, although the actual time period effected is not the same. Minimum losses during the rise time \((t_r)\) are achieved only with a peak gate current \((I_{\text{GM}})\) above 50 amperes, were as the losses during the delay time become negligible with a peak current above 20 amperes. The results indicate an optimum peak gate current \((I_{\text{GM}})\) of 40 amperes should be applied to these devices, which is more than double the figure usually implied in manufactures data [3] for this rating of device.

Some consideration was given to the other principal turn-on parameters, to determine which operating conditions most require the gate pulse to assist the turn-on process. All results indicate that the delay time \((t_d)\) is not significantly affected by the rate of rise of anode current \((\text{di/dt})\) within the range tested. The rise time \((t_r)\) shows a significant increase as the rate of rise of anode current \((\text{di/dt})\) becomes higher. The turn-on energy is also influenced by the rate of rise of anode current \((\text{di/dt})\), with the largest contribution being during the device rise time \((t_r)\). In the 2.5kV devices the energy contribution during the delay time \((t_d)\) is small and almost unaffected by the rate of rise of anode current \((\text{di/dt})\). The peak anode currents \((I_{\text{TMM}})\) shows no significant effect on the turn-on time within the range of measurement, however, it does have an influence on the turn-on losses, most significantly in the 4.5kV device were the higher tail voltage of these devices is a significant factor. The greatest influence would appear to be at lower currents with the energy increase per unit current falling as the current rises.
The supply voltage ($V_D$) has very little influence on the turn-on time, but an appreciable effect on the turn-on losses, principally during the delay time.

As well as the GTO thyristor samples manufactured to a common specification, other larger device types were used in the application measurements. The additional samples were used to verify the results and to expand the range of operating conditions beyond the capability of the smaller test samples.

**Pulse circuit applications.**

The suitability of GTO thyristors to high current pulse applications, as fast turn-on thyristors, has been established, [1]. In general this type of application requires the devices to operate both in series and under very high peak current, with a very fast rate of rise. Some experimental measurements have been conducted both on the common test samples and some larger area devices. The additional samples are of nominal 2000 amperes and manufactured at two different voltage grades (2.5kV and 4.5kV), with both symmetrical as well as anode-shorted structures.

**Test circuit.**

To evaluate the influence of the gate characteristics at a wide range of operating conditions the simple test circuit of figure 7 was constructed. The test circuit comprised of an LC discharge circuit (C2-L2) charged from a 0 to 2000V DC supply via the energy storage circuit C1-L1-R1, where C1>>C2. To obtain a very high rate of rise of anode current (di/dt) the minimum loop inductance L2 is kept very small at <0.1µH, with additional inductance being added for measurements requiring lower values of di/dt. The gate drive circuit comprises an IGBT switch sourced from a variable 0-200V supply, which allows for both a high peak gate current and short gate current rise-time [1]. A typical set of test device wave-diagrams for the pulse circuit are included in figure 8, in this example for a nominal 2000A symmetrical 4.5kV device.

**Experimental results.**

An extensive range of tests were conducted on the various test samples reviewing the influence of both the gate pulse, the anode current and anode-cathode supply voltage. In general the conclusions were similar to those observed in the original evaluation of the 800 ampere devices, but with the modified circuit and larger test devices it was possible to greatly extend the range of conditions of operation, some example results obtained with the test samples follows

Figure 9 & 10 show the influence of the rate of rise of gate current on the turn-on times for the same 2.5kV symmetrical test device used in the results of figures 3 to 6, similar results were obtained with other test samples of both current ratings and all voltage grades. The curves of figures 9 & 10 are given for three gate current rise times of 1, 2 & 3µs, it can be seen that only the delay time ($t_d$) is significantly influenced, with the peak gate current being a more significant factor. The test circuit offers a gate drive with an extended range of peak gate current ($I_{GM}$) than was used in the earlier measurements and it can be clearly seen from figures 9 & 10 that the higher anode current and di/dt of these measurements ($I_{an}=800A$ & di/dt=1kA/µs) increases the influence of the peak gate current on the turn-on time. For an optimum turn-off at a di/dt of 1kA/µs a peak gate current ($I_{GM}$) of 80 amperes is implied for the sample devices.

**Inverter circuit applications.**

Changes in power factor under load conditions in a voltage fed inverter allow for the possibility of anode current rising during any period of the gate forward current pulse, if the gating pulses are not synchronised to the sinusoidally varying current. In order to investigate the significance of the
Figure 11, Delay time vs Peak gate current.

Figure 12, Turn-on energy vs Peak gate current.

Figure 13, Gate trigger delay test circuit.

Test circuit. The basic test circuit comprises of an inductor to control the rate of rise of anode current (di/dt), in series with a thyristor and the GTO thyristor under test. A pulse control circuit allows for adjustment of the delay between the firing of the GTO thyristor gate circuit and the series thyristor Tx, allowing a delay in the application of anode current, after the initiation of the GTO thyristor gate pulse. The GTO thyristor gate drive is of conventional design, except for the inclusion of an adjustable forward gate current (I_G) with a range of 0 to 10 amperes. The series inductor limits the rate of rise of anode current to a few amperes per microsecond, equivalent to the leading edge of the sinusoidal current in the inverter application. Unlike the practical case the test circuit does not allow for the rising anode current to come from the negative half cycle but is initiated from zero current, however this should not interfere with the investigation into the basic principles of the effect. As the GTO thyristor is not turned on from a reverse biased state, there is a snubber discharge through the GTO thyristor when it is initially gated, however this is also not thought to detract from the circuit effects under investigation.

Experimental results. The effect of delayed firing of the series thyristor on the GTO thyristor anode current and voltage is illustrated in figures 14, during the experimental tests three different forms of operation were observed. When sufficient forward gate current (I_G) is supplied to the device a normal current pulse is seen, with voltage rising across the device only when the GTO thyristor is gated off. If the forward gate (I_G) current to the device is reduced then at the start of the rising anode current forward voltage appears across the device, which increases with the reduction of gate current. As the forward gate current is progressively reduced the anode current also falls, the progress of the voltage and current for reducing values of gate current is indicated by the arrows in figure 14. The effect seen is probably due to transistor action taking place in the GTO thyristor, with the device coming out of saturation and operating in what is effectively a linear mode.

Finally it was also observed that the period of delay, after the initial peak gate current pulse (I_ow), before triggering the thyristor Tx, had an influence on the level of gate current required to give normal triggering in the GTO thyristor. The influence of the delay is most clearly seen in figure 15, where the forward gate current (I_G) required to prevent the GTO thyristor from coming out of saturation is plotted against delay time. The delay characteristic was recorded at four different temperatures, to determine the significance of this important parameter and these can be seen as separate lines in the figure.

The measurement of the gate current at four temperatures also allowed for a comparison with the normally measured gate trigger current represented in figure 16, with IGT(1) representing normally measured trigger current and the required current after a delay of 400 microseconds being represented by IGT(2). It can be clearly seen from these results that a higher value of Forward gate current (I_G) than the manufactures data [3] may be required in some inverter applications.

The results for figures 15 & 16 are for a larger area symmetrical 4.5kV, 1200 ampere device, however similar results were obtained for all the samples tested regardless of the manufacturing details.
Series operation.

The series operation of GTO thyristors is a common practice in a number of application areas, some of which have already been considered [1], others of which are both voltage and current fed inverters for medium voltage applications, Saotome & Konishi [4] & Wu & DeWinter [5]. While no specific experimental measurements have been conducted for this type of operation many of the results and conclusions can be directly applied to this type of operation.

In order to safely operate GTO thyristors in series it is necessary to match the devices for the dynamic operation including turn-on, particular attention being required for the delay time. As can be seen from the various results presented in this paper considerable reductions in delay time can be achieved with the use of a peak forward gate current (I_{GM}) greater than that implied in the device manufacturers data. Close scrutiny of the data obtained during the experimental measurements also drew the conclusion that for a particular GTO thyristor type a substantial reduction in the variation of delay time between separate components was found if a high value of peak gate current (I_{GM}) is employed, Wakeman.F & Baker.M [6]. This is well illustrated in figure 17, which shows the reduction of delay time for an increase in gate trigger current in three sample GTO thyristors of identical size, nominal 2000A in the graphical example, but different structures, symmetrical and anode shorted devices at two different voltage grades.

![Figure 17. Influence of the peak gate current on delay time for different device structures.](image)

From the curves of figure 17, for the three different device structures it may be reasonably concluded that the convergence seen in the curves, would be greater enhanced in a single device type. The reduction of variation in the delay time (t_d) when a higher value of peak gate current (I_{GM}) is used, both ensures uniform turn-on of the devices in the series stack and a reduction in the need for the device manufacturer to select devices with similar delay times (t_d).

One additional aspect of the series stack can also be improved with the introduction of an increase in the peak gate current (I_{GM}) [6]. Figure 18 illustrates the effect of a parallel connected turn-on snubber capacitor on the turn-on times of the GTO thyristor, as can be seen the turn-on time is increased by a larger value of capacitor, the example is for symmetrical 2.5kV device with a nominal turn-off current rating of 800A.

![Figure 18. Influence of a turn-on snubber capacitor on the turn-on times.](image)

From the illustration of figure 17 & 18 it is possible to conclude that the value of snubber capacitor may be reduced if an increased value of peak gate current (I_{GM}) is employed, resulting in a faster turn-on time for the series operation switch.

Conclusion

From the experimental results it is possible to draw some conclusions regarding the forward gating requirements of GTO thyristors in specific applications. It is apparent that increasing the peak gate trigger current (I_{GM}) to a value far greater than the figure used in the manufactures rating of the device, may in some applications improve the operational performance. In particular a peak gate current (I_{GM}) as much as four times the normal rating for a particular device type may be applicable in both pulse applications with high anode current di/dt values and applications were more than one device is used in series.

The general reduction in turn-on switching losses associated with the use of a high value of peak gate current (I_{GM}) may also be considered appropriate for devices designed with high blocking voltage capability of 6kV and above, to reduce the inherently high losses of the tail voltage period.

The rate of rise of the peak gate current at device turn-on does not appear to have as much influence on the turn-on as the peak gate current, provided it is in the order of 1 or 2µs.

A higher value of forward gate current (I_G), than implied by the static measurement of gate trigger current (I_{GT}), may be required in some inverter applications where the anode current can rise with some delay after the initial turn-on gate pulse.
References


